Rohan Kalluraya

617-401-6581 rak298@cornell.edu rohankall rohankall

Education

Cornell University, Ithaca, NY **Expected Graduation 2026**

B.S. in Electrical and Computer Engineering, Minor in Computer Science; GPA : 3.88

Relevant Coursework: Embedded Systems, Computer Systems Programming, Circuits, Digital Logic and Computer Organization, Electromagnetism, Machine Learning, Data Structures and Algorithms

Technical Skills

Languages/Database: C, C++, Java, Python, MATLAB, R, Verilog, OCaml, Bash, SQL, Latex Scientific computing
Platforms: Altium, Git, Autodesk Fusion 360, EAGLE, Arduino ESP32
Libraries: Numpy, Matplotlib, Pandas, TensorFlow, PyTorch, HiGHS, JuMP
Awards: National Topper in ICSE Computer Science, Distinction in Euclid and Hypatia Math Contest, National Rank #15 LIMIT Math Exam, National Rank #7 Sridhara National Math Contest

Relevant Experience

Cornell Cup Robotics Project Team **February 2024 – Present**

ECE Subteam Member *Cornell, Ithaca*

- Created environment maps using sensor data for a Bipedal Operations Robot, resulting in path planning time reduction from 10 minutes to 2 minutes using A search* compared to previous methods.
- Developed a series of interconnected circuits on a protoboard, including microcontrollers (Arduino/ESP32) to control the motors and accelerometer sensors for balance feedback, reducing signal processing latency from 500ms to 300ms.
- Used PCB CAD to design a custom breakout shield interfacing with pressure sensors, motor controller output, IMU, and a power + battery management system for seamless hardware integration.
- Integrated a 4000mAh rechargeable Li-ion battery to power the motors, sensors, and control unit, extending operation time from 3 hours to 4 hours and optimizing overall power efficiency, reducing battery drain by 1.5W during active tasks
- Installed a front-facing camera with wide-angle capability to provide real-time visual input. The camera, connected to a Raspberry Pi, enabled object detection and obstacle avoidance using OpenCV for computer vision.

Quality Assurance Intern - BURE Research Program **June 2024 – September 2024**

Software Testing *Cornell, Ithaca*

- Developed a tool for auto-generating inline tests - allowing developers to provide arbitrary inputs and test oracles immediately after target statements for quality assurance. Collaborating with Professor Saikat Dutta.
- Developed scripts to auto-retrieve, instrument and execute 1000 Kaggle Competition Notebooks with 2450 inline tests.
- Carried out intensive debugging operations across all notebooks and meticulously documented findings using Excel.

Deeptek.AI **June 2022 – Jan 2023**

Software Engineering Intern *Pune, India*

- Validated the Convolutional Neural Network (CNN) model's ability to identify Pulmonary Embolisms (PE) from CT scans, increasing diagnostic accuracy by 15% compared to previous methods.
- Conducted statistical analyses on the classification and regression metrics of Deeptek's CNN, ensuring a 98% classification accuracy and a 92% regression accuracy, validating the model's reliability and performance.

AG Diagnostics **June 2022 – September 2022**

Software Engineering Intern *Pune, India*

- Found optimal routes for 4 waste collectors to visit each of 34 centers from the central store of a pathology firm, AG Diagnostics, achieving a 35% transport cost reduction for the firm.
- Collected and analyzed location data from 34 centers, and developed a Mixed Integer Linear Program in Julia to optimize routing efficiency and minimize total transport costs.

Projects

XRP Robot Development | *Embedded Systems, Protoboarding, EAGLE Software* **Feb 2024 – May 2024**

- Debugged the SPI multi-communication software protocol with the RFID Sensor between a RaspberryPi and a Arduino for the XRP Robot. Tested and debugged multiple stacked printed circuit boards (PCBs) with Eagle software.
- Developed and programmed ClawBot, an attachment to the XRP robot, designed to autonomously detect and pick up wooden blocks using a 3D-printed robotic arm, contributing to the robot's operational capabilities during its space mission.

Verilog Single Cycle Processor | *Verilog, Quartus, FPGA* **September 2024 – Present**

- Developed a complete single-cycle microprocessor in Verilog, capable of executing essential instructions including arithmetic, logical, branch, load, and store operations.
- Processor designed to handle 15+ standard instructions, ensuring functional coverage for basic computational tasks.
- Tested the implementation using 5 sample instruction RAMs, verifying the accuracy and performance of the processor in different scenarios.